AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE WRITE INTEGRITY LOGGING (As Amended)

Assignee: Intel Corporation

REMARKS

Page 6

Dkt: 884.905US1 (INTEL)

This communication responds to the Advisory Action mailed on February 15, 2006, and in supplemental to the Amendment filed on January 23, 2006 in response to the Final Office Action mailed on November 21, 2005. Claims 1, 9, 14, and 19 are amended, no claims are canceled, and no claims are added. As a result, claims 1-23 are now pending in this Application.

Declaration

The summary page of the Final Office Action indicated that the Office has objected to the Declaration, and that the objection was explained in the "attached Office Action or Form PTO-152. However, no explanation could be found, and the Applicant is unaware of any reason that an objection would be raised to the Declaration. Accordingly, the Applicant respectfully requests clarification regarding this objection, since nothing was mentioned in the Advisory Action regarding this matter.

§112 Rejections of the Claims

The Advisory Action indicated that the definition of a device option ROM provided by the Applicant was sufficient to overcome the Final Office Action rejection of claim 21 under 35 USC § 112, first paragraph. Therefore, it is assumed that this objection has now been withdrawn.

§103 Rejections of the Claims

Claims 1-4, 6-10, 14, 16 and 19 were rejected under 35 USC § 103(a) as being unpatentable over Sarkozy (U.S. 5,732,238; hereinafter "Sarkozy") further in view of Handy (The Cache Memory Book, Academic Press, 1998; hereinafter "Handy"). Claims 5, 17, 18 and 20 were rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of Lee et al. (U.S. 5,937,433; hereinafter "Lee"). Claims 11 and 23 were rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of Howard (U.S. 6,629,198; hereinafter "Howard"). Claim 12 was rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of

AMENDMENT UNDER 37 C.F.R. 1.116 – EXPEDITED PROCEDURE

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE WRITE INTEGRITY LOGGING (As Amended)

Assignee: Intel Corporation

Heemels (U.S. 5,603,331; hereinafter "Heemels"). Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of Kozierok (PC Guide; hereinafter "PC Guide"). Claim 22 was also rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and Lee and further in view of PC Guide. First, the Applicant does not admit that Sarkozy, Handy, Lee, Howard, Heemels, or PC Guide are prior art and reserves the right to swear behind these references in the future. Second, since a prima facie case of obviousness has not been established as required by M.P.E.P. § 2142, the Applicant respectfully traverses these rejections.

Page 7

Dkt: 884.905US1 (INTEL)

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id*. The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants disclosure. *M.P.E.P.* 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599

AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE WRITE INTEGRITY LOGGING (As Amended)

Assignee: Intel Corporation

F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which notes that the motivation must be supported by evidence in the record.

Page 8

Dkt: 884.905US1 (INTEL)

No proper *prima facie* case of obviousness has been established because (1) combining the references does not teach all of the limitations set forth in the claims, (2) there is no motivation to combine the references, and (3) combining the references provides no reasonable expectation of success. Each of these points will be explained in detail, as follows.

Combining The References Does Not Teach All Claim Limitations.

First, with respect to independent claims 1, 9, 14, and 19, it is admitted in the Office Action that Sarkozy does not disclose "that recording an address of a write operation should be done prior to executing an operating system driver." The Office goes on to assert that "Handy explains that disk caches are often implemented in dynamic RAM using software control." However, this fact alone does not imply any particular actions with respect to the sequencing of disk cache control operations. In fact, the Applicant's representative was unable to find anything within the bounds of Handy to support recording write operation addresses prior to "executing an operating system cache driver," as claimed in independent claims 1, 9, 14, and 19 (claims 14 and 19 have been amended to change the term "booting" to "executing" for consistency with claims 1 and 9, and not for reasons related to patentability). Lee, Howard, Heemels, and PC Guide also fail in this respect. While the Office asserts that "write addresses can be written at any time and the cache driver can be one of many Operating System cache drivers loaded in the system," the existence of such a situation using the cited references has not been demonstrated.

Therefore, no combination of Sarkozy, Handy, Lee, Howard, Heemels, or PC Guide can provide recording write operation addresses prior to "executing an operating system cache driver", as claimed by the Applicant in independent claims 1, 9, 14, and 19, and a *prima facie* case of obviousness has not been established. Further, it is respectfully noted that if an independent claim is nonobvious under 35 USC § 103, then any claim depending therefrom is also nonobvious. *See* M.P.E.P. § 2143.03. Therefore, claims 2-8, 10-13, 15-18, and 20-23 are also nonobvious.

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE WRITE INTEGRITY LOGGING (As Amended)

Assignee: Intel Corporation

There Is No Motivation to Combine the References.

Handy's express concern with cache operational speed (e.g., "This book pertains only to CPU caches and not to disk caches. ... CPU caches operate at such high speed that hardware control must be used, and the cache itself must be implemented in static RAM.) teaches away from using the non-volatile cache technology of Sarkozy. See Handy, pg. xv. Adding any one or more of Lee, Howard, Heemels, and PC Guide does nothing to negate the teaching of Handy.

Page 9

Dkt: 884.905US1 (INTEL)

References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02. The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01.

In this case, Handy teaches that such a combination would *not* be desirable. While the Office asserts that "all caches share many desirable qualities such as speed, data coherence, and fault tolerance," this assertion does nothing to overcome the express teaching of Handy. The use of unsupported assertions in the Office Action does not satisfy the explicit requirements needed to demonstrate motivation as set forth by the *In re Sang Su Lee* court. Therefore, the Examiner appears to be using personal knowledge, and is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Combining the References Provides No Reasonable Expectation of Success.

Implementing a disk cache "in dynamic RAM (DRAM) using software control" as taught by Handy does nothing to promote recording write operation addresses prior to "executing an operating system cache driver", as claimed by the Applicant. Since the Office admits this element is also missing from Sarkovy, combining Handy and Sarkovy provides no reasonable expectation of success with respect to the claimed order of operation. Lee, Howard, Heemels, and PC Guide also fail to add anything to this combination that leads to a reasonable expectation of success with respect to achieving the claimed order of operation.

The Office asserts that "one cannot show nonobviousness by attacking references individually." However, it is respectfully noted that it is the *combination* of Sarkovy and Handy (and/or Lee, Howard, Heemels, and PC Guide) that fails to bring about a reasonable expectation

AMENDMENT UNDER 37 C.F.R. 1.116 – EXPEDITED PROCEDURE

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE WRITE INTEGRITY LOGGING (As Amended)

Assignee: Intel Corporation

Page 10

Dkt: 884.905US1 (INTEL)

of success. This is because the required elements are missing from all of the references, and therefore, no combination of these references would lead to a reasonable expectation of success.

In summary, none of the references teach recording write operation addresses prior to "executing an operating system cache driver," nor an "operating system cache driver associated with the non-volatile cache," as set forth in independent claims 1, 9, 14, and 19. No evidence has been entered in the record to support a need to combine the references (in fact the references teach away from the proposed combinations), and no reasonable expectation of success results from any combination. The requirements of M.P.E.P. § 2142 have not been satisfied, and a prima facie case of obviousness has not been established with respect to these independent claims. All dependent claims are also nonobvious, since claims depending from nonobvious independent claims are also nonobvious. It is therefore respectfully requested that the rejections to claims 1-12, 14-20, and 22-23 under 35 U.S.C. § 103 be reconsidered and withdrawn.

Allowable Subject Matter

Claim 13 was indicated to be allowable if rewritten to overcome the rejection(s) under 35 USC § 112, second paragraph, set forth in the Final Office Action and to include all of the limitations of the base claim and any intervening claims. However, since the Applicant believes all of the claims are in condition for allowance as currently presented, the Applicant respectfully declines to amend claim 13 at this time.

AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE WRITE INTEGRITY LOGGING (As Amended)

Assignee: Intel Corporation

CONCLUSION

The Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney Mark Muller at (210) 308-5677, or the undersigned at (612) 349-9592 to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

ROBERT ROYER ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Attorneys for Intel Corporation P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Page 11

Dkt: 884.905US1 (INTEL)

Date March 16 2006

Ann M. McCrackin

Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this _____ day of March 2006.

Chris Hammond

Signature

Name